CentraleSupélec | université PARIS-SACLAY

CENTRALESUPELEC RECRUTE

Assistant Professor in Design of Secure System-on-Chip for Embedded Artificial Intelligence
CDI de droit public

Context

CentraleSupélec is a public scientific, cultural, and professional institution (EPSCP in French) under the authority of the French ministers for higher education and industry. Its primary missions are training high-level scientific general engineers, engineering and systems sciences research, and executive education. As part of its development, CentraleSupélec is seeking an assistant professor to join the Rennes campus and conduct research at the IETR (Institute of Electronics and Digital Technologies, CNRS UMR-6164) laboratory.

The Rennes campus of CentraleSupélec provides instruction for both the general engineering and specialized engineering curricula through the FISA (Engineering Training under Apprentice Status) and FISE (Engineering Training under Student Status) tracks across all three years of the engineering cycle. Thus, the Rennes campus offers three programs aligned with targeted career profiles: specialized engineering in Electronics, specialized engineering in Digital Systems, and the third-year mention of the general engineering program entitled Num-Vi (Numérique et Vivant).

There are six departments in the IETR laboratory, including the Signal and Communications (SC) department. SIGNAL and ASIC are the two research teams in the SC department. The successful candidate will conduct their research within the ASIC (Architecture, Systems, Infrastructure, and Electronics) team. The ASIC team's research covers the entire spectrum, from the adequacy algorithm architecture of intelligent connected systems to hardware proof-of-concept (hardware realization), with considerations for throughput, power consumption, reliability, and safety.

Education Tasks

The workload associated with the position corresponds to a statutory teaching service, i.e., 192 hours of TD equivalent per year. Teaching activities will be carried out over a broad spectrum, covering the lessons taught

- to students of CentraleSupélec's two specialized engineering programs, "Electronics" and "Digital Systems".
- to students of CentraleSupélec's general engineering program in particular:
  - In the first year of the apprenticeship sector (FISA)
  - In the third year as part of the "Numérique et Vivant" mention.

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These activities will take the following forms:

- in initial training: active participation in the supervision of laboratory work and projects, supervision of tutorials, courses, and monitoring of students (internships, gap year, professionalization contract, etc.)
- In continuing education: tutorials or specialized courses on specific subjects related to the candidate's area of expertise

The subjects taught include skills in low- and high-frequency analog electronics, digital electronics, hardware accelerators for AI, embedded architecture, the design of systems-on-chip, and, more generally, a knowledge of the challenges of the digital transition and technological sovereignty. The candidate must be able to teach in English.

The candidate must demonstrate interdisciplinary openness and contribute to various teaching teams. He/she will have to be a driving force in improving and evolving programs addressing the digital transition issues faced by companies and citizens, under the responsibility of the training department and the various program managers.

Research Mission

The successful candidate will conduct their research within the ASIC research team (https://www.ietr.fr/equipe-asic-architecture-systems-infrastructure-and-electronics) of the IETR (Institute of Electronics and Digital Technologies), CNRS UMR-6164.

The objective of the research activities associated with the position will be to strengthen the design of high-performance, low-power, reliable, and secure intelligent embedded systems. Embedded heterogeneous architectures, hardware optimization techniques (approximate computing, fixed-point conversion, hardware pipelining, etc.), algorithmic optimization techniques, and the integration of artificial intelligence mechanisms will be the main approaches adopted. The person recruited must have the expertise to contribute to the design and implementation of high-performance intelligent embedded systems, with the ambition to offer reliable, secure, innovative, sustainable, and energy-efficient solutions. The application areas are mainly: 5G/6G wireless communication systems.

Candidate Profile

The candidate must hold a thesis in electronics with research on embedded artificial intelligence (design and/or implementation). He/She must be an author or co-author of publications in international journals (the publication requirement will depend on the curriculum vitae and number of years of experience). Furthermore, the person recruited must have a passion for teaching, research, teamwork, and be able to teach in both English and French. Finally, the successful candidate must supervise research work related to the themes of the laboratory's ASIC team.

Selection Procedure

Candidates must send before **April 5th, 2026**, by email only, to the following email address, drh.pole-enseignant@centralesupelec.fr, a file in PDF format including:

- A cover letter
- A detailed CV (teaching experience, research, mobility, publications, etc.)
- A research and teaching project fitting within CentraleSupélec (5 to 10 pages)
- A copy of the identity card or passport
- A copy of the doctoral degree and any document attesting to research supervision experience
- And any documents that attest to previous experience

Application Process

The audition for selected candidates will consist of three stages:

- A presentation of the candidate's academic and professional background, along with their proposed teaching and research project.
- A demonstration lesson in English on a predetermined topic, which will be specified in the audition invitation.
- A discussion with the audition committee.

The allotted time for each stage will be detailed as the candidate advances.

Research and Academic Contacts

- Pr. Amor Nafkha, professor at CentraleSupélec, member of the IETR ASIC team, and co-head of the specialization course "Electronics."
  - Amor.nafkha@centralesupelec.fr

- Pr. Yves Louet, director of the Rennes campus of CentraleSupélec:
  - yves.louet@centralesupelec.fr

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